Drift Chamber Amplifier Discriminator Board
AD_FE-16

User manual

Release #1 (08/03/06)

Prepared by Nikolay Bondar (e-mail: bondar@pnpi.spb.ru)

AD16_H

PNPI
2006

AD_FE-16

Introduction

The Anode Amplifier Discriminator Board AD_FE-16 was designed for amplifying and discriminating anode signals from Drift Chambers (DC). The board is optimized for the PNPI made Hexagonal Drift Chambers. The essential feature of the board is integration of analog part and digitizer with sufficient time resolution (RMS less then 2 ns).

Construction

The AD_FE-16 module consists of a printed board assembled with all its components. The board is splited for two areas – analog and digital. Analog part is closed with a copper shield. Analog area has 16 channel input signal protection networks, two ASDQ ASIC's and attendant components. Input connector is a 17X2 socket. The top row of the input connector is a ground connection; the bottom row has input contacts. Digital part is a 16 channel time digitizer and a serial line interface. Also the digital part serves analog part with threshold voltage and test facility. Output connector RJ45 is used for connecting the board with the Concentrator Board. Power connector is a Molex 3X2 pins.

Circuit diagram

The analog part of the AD_FE-16 module consists of the two ASDQ chips (U1, U2), second stage of input protection network and the ASDQ serving networks.
The input protection network for each channel consists of two stages. The first stage of protection network is located directly on the chamber (at special connection and protection board) and consists of bulk resistor (51ohm) two limiting diodes and second SMD resistor (10 Ohm). The second stage of limiting diodes is located at the AD_FE-16 board after input connector.
Amplifier inputs are connected sensor wires with decoupling capacitors.
To provide stable characteristics of the boards, voltage regulators LT1175 (U3) for -3.1V and TK1230 U4) for +3V are used. Both regulators have a current overflow protection, overheating protection and a power on/off control feature (standby mode). Minimum 2,0V is a "Power-ON" signal. The input power voltage ranges are +4.0V - +5,0V and -4,5V - -5,0V. The output voltages of the regulators are: +3,0+/-0,05V and – 3,1+/-0,1V.

The discriminator threshold control voltages come from digital part of the board via voltage followers (U5 - AD8534). Its range is 0 - 1.0 V. To minimize threshold variation in one board two threshold control voltages (THR1 and THR2) are generating for two ASDQ chips.
The board has an internal test feature. Test signal amplitude levels for odd (TREFO) and even (TREFE) channels are generated at the digital part of the board and go to ASDQ via voltage followers (U5 -AD8534). Test signal width pulses (TSTN and TSTP) also generated at the digital part at the board.
Each ASDQ chip has its individual service network. There is possibility to use BLR monitor by connecting jumpers J7, J8.
. The AD_FE-16 output signals are LVDS compatible.

Digital part is based on FPGA SPARTAN XC3S200 (XILINX). There are Serial Interface, Time-to-Digital Coder with time bin 2,5ns, and threshold control and test facility implemented into this chip.

Application note

As far as the AD_FE-16 board is a computer controllable module it cannot work without interface.

Troubleshooting

All boards after production are carefully tested.
In case of problems:
- Connect board to the interface.
- Switch on power
- Initialize the board
- Check the power voltages (+4,5V – +6,0V), (4,5V – 6,0V) (+3,3V +/-0,05)
- Check the “Power ON” signal (3,0V).
- Check the board consuming current. It should be +4,5 – 140 mA; -4,5V – 160 mA and +3,3V ~500 mA .
- Check the threshold voltage on the board
- Apply external test pulse to the input pin (negative step V~10 mV via capacitor ~3pF – total injecting charge Qin~ 30 fC)

If all voltages are normal, try to watch the output pulse with an oscilloscope (use high impedance probe).
If there is no output pulse on the board, the board needs maintenance.

AD_FE-16 specification

General

Size	86mm x 106mm
Number of channels	16
Input connector	17X2 right angle header
Input connector specification	Top layer all pins are connected to ground. Bottom layer: contact 2 – ground, contacts 4,6, -, 34 are inputs 1-16 corresponding.
Output connector	RJ45-8_VH
Power connector	MINIFIT Molex 43045_6
Contact specification:	Pin 4 - -5V; Pin1 - -5V return (0V) Pin 5 - +5V; Pin2 - +5V return (0V) Pin 6 - +3.3V; Pin 3 +3.3V return (0V)

Power characteristics

Analog positive voltage	+4.0 V – 5V	Current 0.15A
Analog negative voltage	-4.5 V – 5V	Current 0.16A
On board power protection	Fully protected power regulator	
Remote power switch	+3.5 V – power “ON”	
Digital power voltage	+3.3 V +/-0.1V	Current 1A (maximum)

Input characteristics

Input impedance at low frequency	300 Ohm equivalent
Input impedance at high frequency	Rolled off by 30% by 30 MHz
Input DC connection	Capacitor decoupled
Sparkle protection	One stage diode protection (two stages with protection board)
Minimum input signal	5 fC
Maximum input signal	100 fC
Maximum overflow signal	1 pC
Maximum detector capacitance	25 pF

Transfer characteristics

* Amplifier gain	7 mV/fC
Shaping time	6 ns
Detector tail cancellation	Two exponents cancellation circuit
* Amplifier noise Cin=0	0.3 fC
Cin=30 pF	1.2 fC measured
* Threshold control	
Threshold control voltage	0.08 V – 1.0 V
Minimum threshold	5 fC
Maximum threshold	150 fC
Signal propagation time	
** Slewing time	
** Time resolution	
** Dead time	
** Recovery time @10 pC	
@100 pC	
** Maximum test pulse frequency	10 MHz

Output pulse:

Signal levels	LVDS compatible 1.5 mA
Output driver capability	110 Ohm load
Output pulse width	Input pulse width over the threshold (*dE/dx* option disabled)
Leading edge	6 ns
Trailing edge	6 ns

** Cross talk level

Test Pulse parameters

For external test (should be applied directly to the amplifier input):

Negative transition via	3,.3 pF capacitor
Injected charge	Qin(fC)= 3,3(pF)*U(mv)
Minimum pulse amplitude	1 mV (3.3fQ)
Maximum pulse amplitude	500 mV (1.6pQ)
Leading edge	10 ns
Trailing edge	10 ns
Negative pulse width minimum	500 ns

Internal test pulse generator:

Calib. reference for even channels	0 - -3V (-3V – off)
Calib. reference for odd channels	0 - -3V (-3V – off)
Calib. Pulse width	5ns – 15ns
Calib pulse amplitude	0.6V (complementary levels -0.2V - -0.6V)

Test pulse generator should be calibrated

Notes:

*) Parameters are tested for each board.

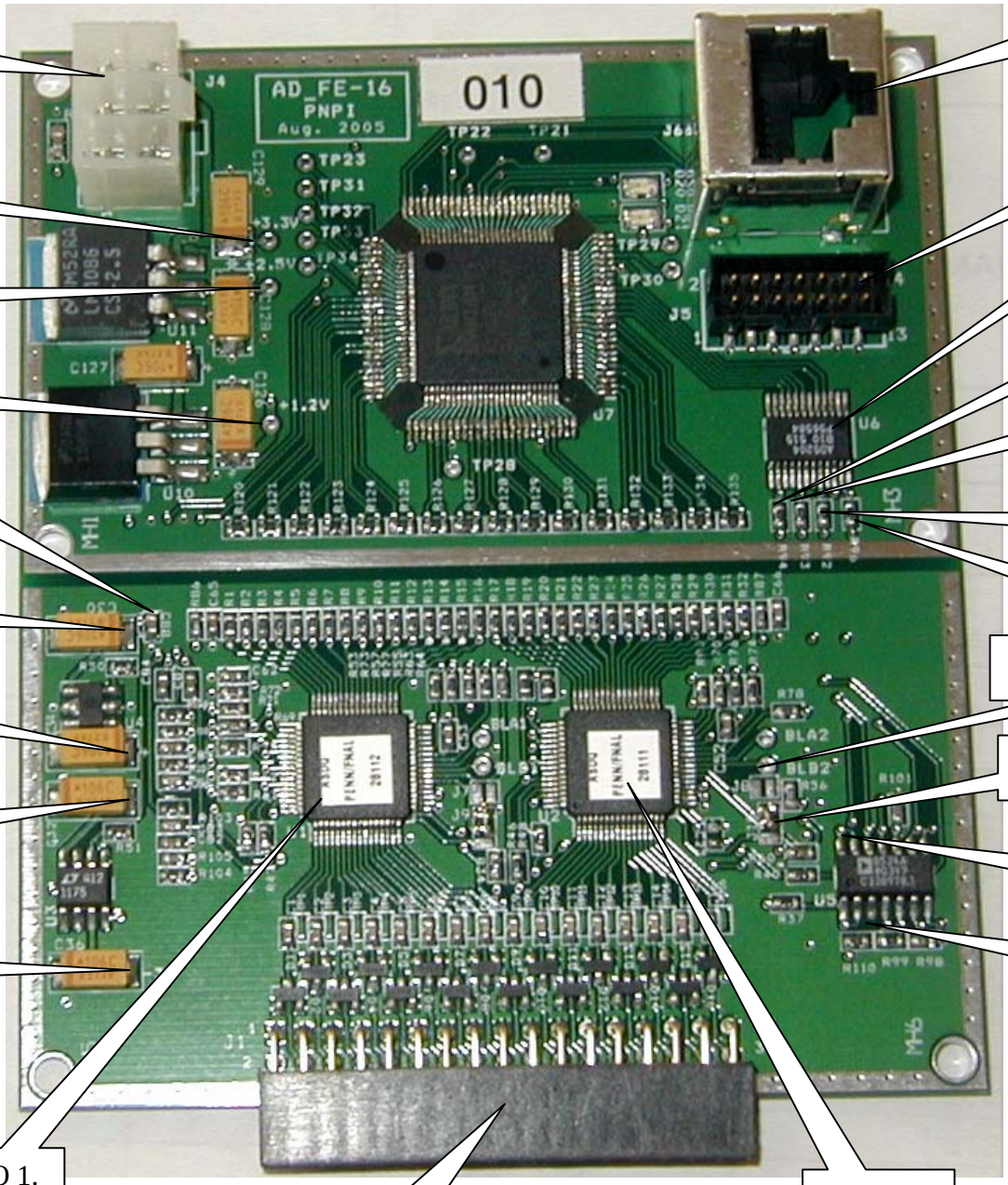
**) Parameters should be tested

ASDQ chip pin specification

Pin	Name	Nominal	Description	Comments
1	IN1A	0.69V =/- 003V	Ch1 Negative going input	
2	IN1B	0.69V =/- 003V	Ch 1 Positive going input	
3	IN2A	0.69V =/- 003V	Ch2 Negative going input	
4	IN2B	0.69V =/- 003V	Ch2 Positive going input	
:	:	:	:	
15	IN8A	0.69V =/- 003V	Ch8 Negative going input	
16	IN8B	0.69V =/- 003V	Ch8 Positive going input	
17	AGND	0	Preamplifier reference	Ground connected to detector
18	AGND	0	Preamplifier reference	Ground connected to detector
19	SUBA	-3.1V+/- 0.1V	Analog Substrate,	Analog minimum voltage
20	VPP	-1.1V	Input protection raile	
21	VCP	+3.0V+/- 0.1V	Preamplifier supply	
22	ATTN	0	Attenuate input by 2, (NO att - V=0	Attenuation is Off (Max. Gain)
23	IBLRM		BLR monitor current reference	Normal - not connected
24	BLB	0	BLR monitor A	Disabled
25	BLA	0	BLR monitor B	Disabled
26	VES	- 3.07V	Shaper&BLR	
27	QTHR	-1.59V	Trailing edge tracking control	
28	ID	+0.68V+/-0.02V	Output current reference	
29	VED	-3.03V	Discriminator dE/dx	
30	VCD	+2.92V	Discriminator dE/dx & Driver	
31	DGND	0	Discriminator &dE/dx ground	
32	VEDR	-2.88V	Driver supply	
33	D8B	1.24V	Ch8 Driver out negative going	
34	D8A	0.75V	Ch8 Driver out positive going	
35	D7B	1.24V	Ch7 Driver out negative going	
35	D7A	0.75V	Ch7 Driver out positive going	
:	:	:	:	
47	D1B	1.24V	Ch1 Driver out negative going	
48	D1A	0.75V	Ch1 Driver out positive going	
49	VEDR	-2.88V	Driver supply	
50	AN3V	-3.2V	Analog negative power	Here -3.1V +/- 0.15V
51	VCD	+2.92V	Discriminator dE/dx & Driver	
52	QEN	+2.94V	dE/dx enable (+3V= Off)	dE/dx disabled
53	QDR	-2.23V	dE/dx cup drain ref (-3v = Off)	dE/dx disabled
54	VED	-3.0V	Discriminator dE/dx	
55	DTHR	+0.17V	Tracking Discriminator Thershold	
56	VCS	+2.94V		
57	IBLR	-0.76V	BLR current reference	
58	TREFE	-3.0V	Calib ref for even channels (-3V= 0ff)	Normal – Off
59	TREFO	-3.0V	Calib ref for odd channels (-3V= 0ff)	Normal – Off
60	TSTP	-0.5V	Positive going calib pulse edge	
61	TSTN	-0.29V	Negative going calib pulse edge	
62	AN3V	-3.20V	Analog Negative Voltage	
63	AGND	0	Preamplifier reference	Ground connected to detector
64	AGND	0	Preamplifier reference	Ground connected to detector

AD_FE-16

Top view.



Power connector.

+3.3V point

+2.5V point

+1.2V point

Power "ON" voltage

+4.5V point

+3V point

-4.5V point

-3V point

Interface connector

JTAG connector

DAC

-TREFO

Thr 2

Thr 1

-TREFE

BLR monitor ON

Attenuation X2

Threshold 2

Threshold 1.

ASDQ 1.

Input connector.

ASDQ 2.

Bottom view